Answer Key: Assistant Professor (VLSI Design & Tech.)

Q No	Key
1	B
2	D
3	B
4	A
5	D
6	C
7	A
8	B
9	**C**
10	A
11	B
12	D
13	B
14	D
15	D
16	A
17	D
18	C
19	B
20	B
21	B
22	B
23	C
24	D
25	D

Q No	Key
26	A
27	D
28	A
29	C
30	C
31	D
32	C
33	C
34	A
35	A
36	B
37	C
38	C
39	A
40	B
41	B
42	D
43	A
44	D
45	A
46	B
47	C
48	B
49	D
50	B

Test Booklet Series

A

Test Booklet No.

Test Booklet for the Post of

Assistant Professor VLSI Design & Technology

Name of Applicant .... Answer Sheet No. ....

Applicant ID/Roll No. : .... Signature of Applicant : ....

Date of Examination: ....

Signature of the Invigilator(s)

1. ....

Time of Examination : ....

2. ....

Duration : 1 Hour] **[Maximum Marks : 50**

IMPORTANT INSTRUCTIONS

(i) The question paper is in the form of Test-Booklet containing **50 (Fifty)** questions. All questions are compulsory. Each question carries four answers marked (A), (B), (C) and (D), out of which only one is correct. Choose the correct option or the most appropriate option.

(ii) On receipt of the Test-Booklet (Question Paper), the candidate should immediately check it and ensure that it contains all the pages, i.e., **50** questions. Discrepancy, if any, should be reported by the candidate to the invigilator immediately after receiving the Test-Booklet.

(iii) A separate Answer-Sheet is provided with the Test-Booklet/Question Paper. On this sheet there are **50** rows containing four circles each. One row pertains to one question.

(iv) The candidate should write his/her Application ID/Roll number at the places provided on the cover page of the Test-Booklet/Question Paper and on the Answer-Sheet and NOWHERE ELSE.

(v) No second Test-Booklet/Question Paper and Answer-Sheet will be given to a candidate. The candidates are advised to be careful in handling it and writing the answer on the Answer-Sheet.

(vi) For every correct answer of the question **One (1) mark will be awarded.** There will be negative marking and 1/4 (0.25) mark will be deducted for every incorrect answer.

(vii) Marking shall be done only on the basis of answers responded on the Answer-Sheet.

(viii) To mark the answer on the Answer-Sheet, candidate should **darken** the appropriate circle in the row of each question with Blue or Black pen.

(ix) For each question only **one** circle should be **darkened** as a mark of the answer adopted by the candidate. If more than one circle for the question are found darkened or with one black circle any other circle carries any mark, the answer will be treated as incorrect.

(x) The candidates should not remove any paper from the Test-Booklet/Question Paper. Attempting to remove any paper shall be liable to be punished for use of unfair means.

(xi) Rough work may be done on the blank space provided in the Test-Booklet/Question Paper only.

(xii) *Mobile phones (even in Switch-off mode) and such other communication/programmable devices are not allowed inside the examination hall.*

(xiii) No candidate shall be permitted to leave the examination hall before the expiry of the time.

DO NOT OPEN THIS QUESTION BOOKLET UNTIL ASKED TO DO SO.

General Physical constants, if not provided in the question :

Planks constant, $h = 4.14 \times 10^{-15}$ eV-sec, 6.626×10^{-34} joule-sec

Si Intrinsic carrier concentration, $n_i = 1.45 \times 10^{10}$ cm^{-3}

Electron mass, $m_0 = 9.108 \times 10^{-31}$ kg

Speed of light in vacuum, $C = 3 \times 10^{8}$ m/sec

Relative permittivity of air = 1

Permittivity of free space, $\varepsilon_0 = 8.85 \times 10^{-12}$ farad/m

Relative permeability of air = 1.257×10^{-6} H/m

Electronic charge, $q = 1.6 \times 10^{-19}$ C

Boltzmann Constant, $k = 1.380649 \times 10^{-23}$ joule K^{-1}

1. As MOS devices are scaled to smaller dimensions, gate oxides must be reduced in thickness. As the gate oxide thickness decreases, the MOS devices become _______________ to sodium contamination.
   (A) Not affected, not prone to sodium contamination, and balanced by other gate oxide charges
   (B) Become less sensitive as oxide thickness decreases.
   (C) Become highly sensitive as oxide thickness decreases.
   (D) Increases the threshold of the MOS cap.

2. In a particular positive resist process exposed with e-beam, it is sometimes noticed that there is difficulty developing away the last few hundred angstroms of resist in exposed areas. Suggest a best possible solution of this problem, without effecting the critical dimension.
   (A) Apply the low exposure dose, with low acceleration voltage.
   (B) Apply the reduced resist development time, and optimize post exposure bake.
   (C) Apply anti reflecting coating over the resist.
   (D) Apply short pulse O_2 plasma results in descum.

3. In a small MOS device, there may be a statistical variation in V_T due to differences in fixed charges from one device to another. In a 0.13 μm technology minimum device (gate oxide area = 0.1 μm × 0.1 μm) with a 2.5 nm gate oxide, what would be the threshold voltage be for devices with 4 fixed charge in the gate oxide, if carrier charge is 1.6×10^{-19}?
   (A) 1.1 mV (B) 4.6 mV
   (C) 3.2 mV (D) 1 V

4. Under what conditions is the thermal growth rate of SiO_2 over perfectly cleaned Si wafer is linearly proportional to time? Where D = Diffusivity, k_s = Surface oxidation reaction rate constant, X_O = Oxide depth.

   (A) The oxide growth is in the linear regime for the low oxide thickness, below 200 nm, and when $k_S X_O/D << 1$.

   (B) The oxide growth is in the linear regime for large values of the oxide thickness, above 500 nm, and when $k_S X_O/D << 1$.

   (C) The oxide growth is in the linear regime for the low oxide thickness, below 200 nm, and when $k_s X_O/D >> 1$.

   (D) The oxide growth is in the linear regime for large values of the oxide thickness, above 500 nm, and when $k_S X_O/D >> 1$.

5. A process engineer on the day shift started a boron isolation diffusion for a structure in which the boron diffusion needs to penetrate completely through a 1 μm thick N-type epitaxial layer that is lightly doped with phosphorus ($N_D = 1 \times 10^{15}$ cm^{-3}) on a P type substrate ($N_A = 1 \times 10^{14}$ cm^{-3}). The purpose of the diffusion is to provide isolation between different N-type regions. The day shift engineer left no information on what he or she did, what should he do best for a quick estimation of the job done without much damaging the sample.

   (A) Check the resistivity by hot probe method.

   (B) Take the IV measurement by two probes and deduce the resistivity by slope.

   (C) Fabricate a hall bar pattern and test the resistivity by Hall method.

   (D) Check the resistivity by van der pauw method.

6. Suggest a best way to decrease the asymmetry deposition over the wafer in sputter deposition.

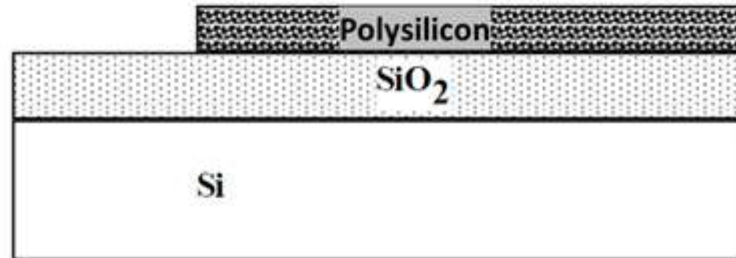
   (A) The target size can be narrowed

   (B) Decrease the spacing between target and wafer.

   (C) Increase the pressure during sputter deposition.

   (D) Increase the temperature during sputter deposition.

7. A resistor for an analog integrated circuit is made using a layer of deposited polysilicon 0.5 μm thick, as shown below. The doping the polysilicon is 1×10^{16} cm^{-3}. The carrier mobility $\mu = 100$ cm^2 V^{-1} sec^{-1} is low because of scattering at grain boundaries. If the resistor has L = 100 μm, W = 10 μm, what is its resistance in Ohms?



(A) 1.25 MΩ (B) 0.5 MΩ

(C) 1.5 MΩ (D) 0.1 MΩ

8. An NMOS transistor is being built and an ion implantation is done after the gate oxide is grown and before the gate polysilicon deposition, in order to adjust the threshold voltage by +1 volt. Calculate the dose/cm^2 of the dopant if the oxide thickness is 10 nm.

(A) 4.51×10^{16} (B) 2.16×10^{12}

(C) 3.50×10^{18} (D) 4.51×10^{14}

9. Consider a piece of pure silicon 100 μm long with a cross-sectional area of 1 μm^2, having overall mobilities of 1000 cm^2 $v^{-1} sec^{-1}$. How much current would flow through this "resistor" at room temperature in response to an applied voltage of 2 volt?

(A) 1.21 pA (B) 2.42 pA

(C) 4.64 pA (D) 5.21 pA

10. A state-of-the-art NMOS transistor might have a drain junction area of 0.5 × 0.5 μm. Calculate the intrinsic fermi potential associated with this junction. The applied reverse bias of 2 volts exists at the junction. Assume the drain region is very heavily doped 1×10^{20} cm^{-3} and the substrate doping is 1×10^{16} cm^{-3}.

(A) 934 mV (B) 620 mV

(C) 500 mV (D) 320 mV

11. When the gate-to-source voltage (V_{GS}) of a MOSFET with threshold voltage of 400 mV, working in saturation is 900 mV, the drain current is observed to be 1.5 mA. Neglecting the channel width modulation effect and assuming that the MOSFET is operating at saturation, the drain current for an applied V_{GS} of 1400 mV is

(A) 0.5 mA (B) 6.0 mA

(C) 4.0 mA (D) 3.5 mA

12. The electron concentration in a sample of doped n-type silicon at 300 K varies linearly from $10^{17}/cm^3$ at x = 0 to $6 \times 10^{16}/cm^3$ at x = 2 μm. Assume a situation that electrons are supplied to keep this concentration gradient constant with time. If electronic charge is 1.6×10^{-19} C and the diffusion constant $D_n = 35$ cm^2/s, the current density in the silicon, if no electric field is present is

(A) +112 A/cm^2 (B) –112 A/cm^2

(C) +1120 A/cm^2 (D) –1120 A/cm^2

13 At 300 K, for a diode current of 1 mA, a certain germanium diode requires a forward bias of 0.1435 V, whereas a certain silicon diode requires a forward bias of 0.718 V. Under the conditions state above, the closest approximation of the ratio of reverse saturation current in germanium diode to that in the silicon diode is

(A) 1×10^2 (B) 4×10^3

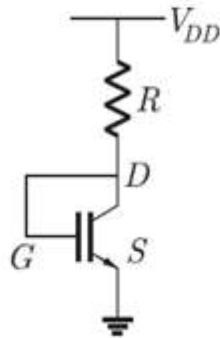
(C) 5×10^3 (D) 8×10^3

14. For a BJT the common base current gain 0.98 and the collector base junction reverse bias saturation current $I_{co} = 0.6$ mA. This BJT is connected in the common emitter mode and operated in the active region with a base drive current $I_B = 20$ μA. The collector current I_c for this mode of operation is

(A) 0.98 mA (B) 0.99 mA

(C) 1.0 mA (D) 1.01 mA

15. For the n-channel MOS transistor shown in the figure below, the threshold voltage V_{Th} is 0.8 V. Neglect channel length modulation effects. When the drain voltage $V_D = 1.6$ V, the drain current I_D was found to be 0.5 mA. If V_D is adjusted to be 2 V by changing the values of R and V_{DD}, the new value of I_D is

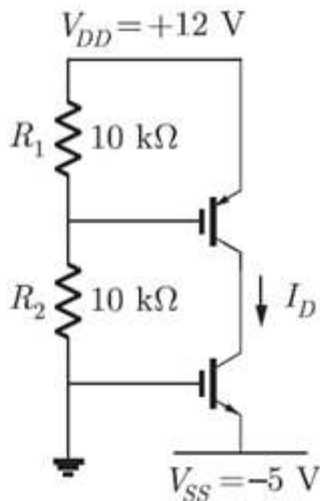


(A) 0.625 mA
(B) 0.75 mA
(C) 1.5 mA
(D) 1.125 mA

16. For the MOSFETs shown in the figure, the threshold voltage $V_t = 2$ V and

$$K = \frac{1}{2}\mu C_{ox}\frac{W}{L} = 0.1\ \text{mA/V}^2.$$

The value of I_D (in mA) is ____.



(A) 0.9 mA
(B) 1 mA
(C) 1.1 mA
(D) 2.9 mA

17. Calculate the overdrive voltage for NMOS transistor with I_D = 1 μA, I_{VT} = 0.1 μA, and $V_{DS} >> V_T$. Device parameters are W = 10 μm, L = 1 μm, n = 1.5, K' = 200 $\mu A/V^2$ and t_{ox} =100 Å. Assume the temperature is 27°C.

(A) 8 mV (B) 16 mV

(C) 64 mV (D) 32 mV

18. The outputs of two systems S1 and S2 for same input $x[n] = e^{i\pi n}$ are 1 and $(-1)^n$, respectively. Which of the following statements are correct.

(A) Both S1 and S2 are linear time invariant systems.

(B) S1 is linear time invariant but S2 is not linear time-invariant.

(C) S1 is not linear time invariant but S2 is linear time invariant

(D) Neither S1 nor S2 is linear time-invariant.

19. A system is defined by its impulse response $h(n) = 2^n u[n-2]$. The system is :

(A) Stable and causal (B) Causal but not stable

(C) Stable but not causal (D) Unstable and noncausal

20. A Si pn Junction diode under reverse bias has depletion width of 10 μm. The relative permittivity of Si (ε_r) = 11.7 and permittivity of free space (ε_0) is 8.85×10^{-12} F/m. The depletion capacitance of the diode per square meter is :

(A) 100 μF (B) 10 μF

(C) 1 μF (D) 20 μF

21. If the emitter resistance in a common emitter voltage amplifier is not bypassed, it will

(A) Reduced both the voltage gain and the input impedance

(B) Reduce the voltage gain and increase the input impedance

(C) Increase the voltage gain and reduce the input impedance.

(D) Increase both the voltage gain and the input impedance.

22. To obtain very high input and output impedance in a feedback amplifier, the topology mostly used is :

(A) Voltage series (B) Current series

(C) Voltage shunt (D) Current shunt

23. The slope of the I_D vs V_{GS} curve of an n-channel MOSFET in linear regime is $10^{-3}\ \Omega^{-1}$ at $V_{GS} = 0.1$ V. For the same device, neglecting the channel length modulation, the slope of the $\sqrt{I_D}$ vs V_{GS} curve (in $\sqrt{A}$ / V) under saturation regime is approximately.

(A) 0.05 (B) 0.06

(C) 0.07 (D) 0.08

24. Consider a chip design using 10 mask levels. Suppose that each mask can be made with 98% yield. Determine the worst-case composite mask yield for the set of 10 masks.

(A) 98% (B) 49%

(C) 48.8% (D) 81.7%

25. Calculate the W/L of MOSFET in the resistive load inverter configuration with load resistance, R = 1 kΩ such that $V_{OL} = 0.6$ V. When an enhancement-type nMOS driver with following parameters $V_{DD} = 5.0$ V, $k' = 22.0\ \mu A/V^2$, $V_T = 1.0$ V. Condition: the driver transistor operates in the linear region, i.e. $V_{OUT} = V_{OL}$, $V_{IN} = V_{DD} = 5.0$ V.

(a) 45.05 (b) 30.03

(c) 22.5 (d) 90.1

26. What of the following causing the charge sharing problem in domino CMOS VLSI circuits.

(A) Charge sharing between output capacitance and an intermediate node capacitance.

(B) Charge sharing between input capacitance and output load capacitance.

(C) Charge sharing between input capacitance and an intermediate node capacitance

(D) Charge sharing with pMOS pull up transistor to force the node remain low.

27. The nMOS and pMOS transistors in a CMOS inverter have the following parameters : V_{to} = 1.0 V for both nMOS and pMOS transistors, $\lambda = 0.0\ V^{-1}$. The CMOS inverter is designed with $(W/L)_p = 20$ and $(W/L)_n = 10$, and its capacitive load is 2 pF. Calculate the average power dissipation in the inverter when its input signal is a rectangular pulse with 100 ns period which swings 5 V and 0 V. It is assumed that load capacitance and parasitic capacitances connected to the drain node.

(A) 0.25 mW (B) 1 mW

(C) 2 mW (D) 0.5 mW

28. A BJT transistor has $\alpha_F = 0.99$ and $\alpha_R = 0.2$. Calculate the collector junction reverse saturation current. when its emitter junction reverse saturation current is 10^{-14} A.

(A) 4.95×10^{-14} A (B) 2.48×10^{-14} A

(C) 1.24×10^{-14} A (D) 0.20×10^{-14} A

29. The bonding pad in I/O circuit are implemented in the topmost metal layer with a dimension of 75 μm × 75 μm. If the separation of the topmost metal layer with SiO_2 from the common substrate layer (ground plane) is 1 μm. Calculate the capacitance (parasitic) of the bonding pad?

(A) 0.38 pF (B) 0.76 pF

(C) 0.19 pF (D) 0.152 pF

30. Following entity represents a ______________ circuit.

```
ENTITY my_circuit is
PORT (a, b : IN STD_LOGIC_VECTOR (3downto 0);
x : OUT STD_LOGIC_VECTOR (3downto 0);
y : OUT STD_LOGIC;
END my_circuit;
```

(A) Serial Adder (B) Half Adder

(C) Parallel adder (D) Full Adder

31. What is the correct method to declare a SIGNED type signal ‘x’?

(A) SIGNAL x : IN SIGNED_VECTOR (7 DOWN TO 0)

(B) SIGNAL x : IN SIGNED

(C) SIGNAL x : OUT SIGNED

d) SIGNAL x : IN SIGNED (7 DOWN TO 0)

32. Which of the following is not defined by the entity?

(A) Direction of the signal

(B) Different ports

(C) Behavior of the signal

(D) Name of the signal

33 What will be the value of the following variables after MOD operations?

X = 5 MOD 3;

Y = –5 MOD 3;

Z = 5 MOD –3;

(A) X = 2, Y = –1 and Z = 2

(B) X = 2, Y = –2 and Z = –2

(C) X = 2, Y = 1 and Z = –2

(D) X = 2, Y = –2 and Z = 1

34. In most synthesis tools, only generic of types ___________ are supported

(A) INTEGER

(B) REAL

(C) STD_LOGIC

(D) BIT_VECTOR

35. Which of the following is true about guarded blocks?

(A) Guarded blocks can have both guarded as well as unguarded statements

(B) Guarded blocks can have only guarded statements

(C) Guarded blocks are executed when guarded expression is false

(D) Guarded expression can have BIT type

36. Which type of simulator/s neglect/s the intra-cycle state transitions by checking the status of target signals periodically irrespective of any events?

(A) Event-driven Simulator (B) Cycle-based Simulator

(C) Both (A) and (B) (D) None of the above

37. In signal integrity, which noise/s occur/s due to impedance mismatch, stubs, vias and other interconnection discontinuities?

(A) Power/Ground Noise (B) Crosstalk Noise

(C) Reflection Noise (D) All of the above

38. If A = 1'b1, B = 2'b01, C = 2'b10 then Y = {A, B[1], C[0]} will result in

(A) 5'b10110 (B) 3'b111

(C) 3'b100 (D) 3'b000

39. Which level of routing resources are supposed to be the dedicated lines allowing output of each tile to connect directly to every input of eight surrounding tiles?

(A) Ultra-fast local resources (B) Efficient long-line resources

(C) High speed, very long-line resources (D) High performance global networks

40. In high noise margin (NMH), the difference in magnitude between the maximum HIGH output voltage of driving gate and the maximum HIGH voltage is recognized by the _________gate.

(A) Driven (B) Receiving

(C) Transmission (D) All of the above

41. Maze routing is also known as ________

(A) Viterbi's algorithm (B) Lee/Moore algorithm

(C) Prim's algorithm (D) Quine-McCluskey algorithm

42. The lattice constant of Ge at room temperature is $a = 5.65 \times 10^{-8}$ cm. Determine the number of Ge atoms/cm^3.

(A) 2.22×10^{22} atoms/cm^3 (B) 8.88×10^{22} atoms/cm^3

(C) 6.66×10^{22} atoms/cm^3 (D) 4.44×10^{22} atoms/cm^3

43. A planer P^{++}-n Si step junction diode with an n-side doping of ND = 10^{15}/cm^3, breakdown voltage of 320 V and T = 300 K, determine the depletion width at the breakdown voltage.

(A) 20.4 μm (B) 10.2 μm

(C) 40.8 μm (D) 5.021 μm

44. A semiconductor fabrication facility manufactures 1000 wafers weekly. It's estimated that each wafer holds 100 chips, each potentially yielding $50 in revenue if functional. Presently, the chip yield stands at 50%. Enhancing the yield would substantially boost profits, as all 100 chips are produced regardless of functionality. What increase in yield is required to generate a yearly profit surge of $10,000,000?

(A) 5.5% (B) 15.4%

(C) 2.25% (D) 7.7%

45. Assume there are no clear choices for lithography systems beyond optical projection tools based on 193-nm ArF excimer lasers. One possibility is an optical projection system using a 157-nm F2 excimer laser. a. Assuming a numerical aperture of 0.8 and k1 = 0.75, what is the expected resolution of such a system using a first order estimate of resolution?

(A) 147 nm (B) 165 nm

(C) 294 nm (D) 73.5 nm

46. The circle can rotate clockwise and back. Use minimum hardware to build a circuit to indicate the direction of rotating.?

(A) Two D flip flop and one Sensors (B) Two sensors and D flip flop

(C) One Sensor only (D) One sensor and D flip flop

47. Which of the following is not a way to reduce clock skew to zero?

(A) Use pure H tree

(B) clock layout strategies

(C) process variations in R and C across the chip

(D) buffering, and clock gating

48. If x = 6’b101110, then x << 2 will result in

(A) 6’b101011

(B) 6’b101100

(C) 6’b001010

(D) None of the above

49. What is the SWAMI in VLSI, and what it signifies?

(A) SWAMI stands for Silicon Wafer Advanced Manufacturing Integration, optimizing chip fabrication processes.

(B) SWAMI refers to Silicon Wafer Analysis for Microchip Integration, aiding in chip processing design.

(C) SWAMI represents Silicon Wafer Analysis Management Interface, enhancing integration efficiency.

(D) SWAMI denotes Side Wall Masked Isolation, utilized for reducing bird’s beak effect.

50. In a CMOS inverter circuit configuration (PMOS and NMOS transistors connected in series with common input V_{in}) with V_{in} = 2.5 V, V_{DD} = 5 V. If the transconductance parameters of the NMOS and PMOS are $k_n = k_p = 20\frac{\mu A}{V^2}$, $V_{Tn} = V_{Tp}$ = 1 V the Current I flowing through the PMOS to NMOS is

(A) 0 μA

(B) 45 μA

(C) 25 μA

(D) 90 μA

ROUGH WORK

ROUGH WORK